Amendments to the Claims

This listing of claims replaces all prior versions, and listings, of claims in the above-identified application:

Listing of Claims

1-22. **(CANCELED)**

23. **(CURRENTLY AMENDED)** A semiconductor device structure, the structure comprising:

a substrate assembly including a surface; and

a conformal chemical vapor deposited barrier layer over at least a portion of the surface, wherein the barrier layer is formed of a simultaneously co-deposited platinum(x):ruthenium alloy, where x is in the range of about 0.60 to about 0.995.

24. **(ORIGINAL)** The structure of claim 23, wherein x is in the range of about 0.90 to about 0.98.

25. **(ORIGINAL)** The structure of claim 24, wherein x is about 0.95.

26. **(ORIGINAL)** The structure of claim 23, wherein the portion of the surface is a silicon containing surface.

27. **(CURRENTLY AMENDED)** A capacitor structure comprising:

a first electrode;

a dielectric material on at least a portion of the first electrode; and

a second electrode on the dielectric material, wherein at least one of the first electrode and second electrode comprises a chemical vapor deposited barrier layer of a simultaneously co-deposited platinum(x):ruthenium alloy.

28. **(ORIGINAL)** The structure of claim 27, wherein x is in the range of about 0.60 to about 0.995.

29. **(ORIGINAL)** The structure of claim 28, wherein x is in the range of about 0.90 to about 0.98.

30. **(CURRENTLY AMENDED)** The structure of claim 27, wherein at least one of the first electrode and second electrode comprises the barrier layer of the simultaneously co-deposited platinum(x):ruthenium alloy and one or more additional conductive layers.

31. **(PREVIOUSLY PRESENTED)** The structure of claim 30, wherein the one or more additional conductive layers are formed from materials selected from the group of metals and metal alloys; metal and metal alloy oxides; metal nitrides; and metal silicides.

32. **(CURRENTLY AMENDED)** A memory cell structure comprising:

a substrate assembly including at least one active device; and

a capacitor formed relative to the at least one active device, the capacitor comprising at least one electrode including a chemical vapor deposited barrier layer formed of a simultaneously co-deposited platinum(x):ruthenium alloy.

33. **(CURRENTLY AMENDED)** The structure of claim 32, wherein the capacitor includes:

a first electrode formed relative to a silicon containing region of the at least one active device;

a dielectric material on at least a portion of the first electrode; and

a second electrode on the dielectric material, wherein the first electrode comprises the barrier layer formed of the simultaneously co-deposited platinum(x):ruthenium alloy.

34. **(CURRENTLY AMENDED)** The structure of claim 33, wherein the first electrode comprising the barrier layer formed of the simultaneously co-deposited platinum(x):ruthenium alloy includes one or more additional conductive layers.

35. **(ORIGINAL)** The structure of claim 33, wherein x is in the range of about 0.60 to about 0.995.

36. **(ORIGINAL)** The structure of claim 35, wherein x is in the range of about 0.90 to about 0.98.

37. **(CURRENTLY AMENDED)** An integrated circuit structure comprising:

a substrate assembly including at least one active device; and

an interconnect formed relative to the at least one active device, the interconnect including a conformal barrier layer formed of a simultaneously co-deposited platinum(x):ruthenium alloy.

38. **(ORIGINAL)** The structure of claim 37, wherein x is in the range of about 0.60 to about 0.995.

39. **(ORIGINAL)** The structure of claim 38, wherein x is in the range of about 0.90 to about 0.98.

40. **(CANCELED)**

41. **(PREVIOUSLY PRESENTED)** The structure of claim 23, wherein the at least a portion of the surface defines a small high aspect ratio opening.

42. **(PREVIOUSLY PRESENTED)** The structure of claim 23, wherein a thickness of the barrier layer is in a range of about 10 Å to about 10,000 Å.

43. **(PREVIOUSLY PRESENTED)** The structure of claim 42, wherein the thickness of the barrier layer is in a range of about 100 Å to about 500 Å.

44. **(PREVIOUSLY PRESENTED)** The structure of claim 23, wherein the substrate assembly comprises at least one active device.

45. **(PREVIOUSLY PRESENTED)** The structure of claim 37, wherein the barrier layer comprises a chemical vapor deposited barrier layer.

46. **(PREVIOUSLY PRESENTED)** The structure of claim 37, wherein the substrate assembly comprises a small high aspect ratio opening, and further wherein the interconnect is formed in the small high aspect ratio opening relative to the at least one active device.

47. **(PREVIOUSLY PRESENTED)** The structure of claim 37, wherein a thickness of the barrier layer is in a range of about 10 Å to about 10,000 Å.

48. **(PREVIOUSLY PRESENTED)** The structure of claim 47, wherein the thickness of the barrier layer is in a range of about 100 Å to about 500 Å.

49. **(PREVIOUSLY PRESENTED)** The structure of claim 39, wherein x is about 0.95.